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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,035	05/20/2004	Kazuya Fukuhara	67160-019	7029

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/849,035	FUKUHARA, KAZUYA	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *8-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group I in the reply filed on 3/22/2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al., US patent No. 4,831,424.

Regarding claim 1, Yoshida teaches a MOSFET (fig. 1), comprising: a semiconductor substrate having one of main surface (top surface of the substrate1) and the other main surface (bottom surface of the substrate 1) opposite to each other, the semiconductor substrate having a source electrode (S) and a gate electrode (G) provided on the one main surfaces and a drain electrode (D) provided on the other main surface; a source terminal layer (the terminal above the source electrode) disposed on the one main surface and joined to the source electrode (S); a gate terminal layer (the terminal above the gate electrode) disposed on the one main surface and joined to the gate electrode (G); and a drain terminal layer (the terminal above the drain electrode D)

disposed on the other main surface and joined to the drain electrode (D); wherein the source terminal layer and the gate terminal layer are respectively disposed on the one main surface with such sizes as to fall within the area of the one main surface (refer to fig. 1), and the drain terminal layer is disposed with such a size as to fall within the area of the other main surface (refer to fig. 1).

The limitation of power MOSFET is not given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Wang et al. US patent No. 5,866,947.

Regarding claim 2, Yoshida teaches substantially the entire claimed structure of claim 1 above except stating that the source terminal layer, the gate terminal layer, and

the drain terminal layer are respectively jointed to the respective main surfaces with conductive adhesives.

The use of conductive adhesives is conventional in the art and also taught by Wang (col. 5, lines 11-21 and fig. 2) the use of adhesion layer (10) in the structure of forming source/drain contact.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the adhesive layer taught by Wang in the structure of Yoshida in order to improve contact resistance.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Herbert, US patent No. 3,577,019.

Regarding claim 3, Yoshida teaches the entire claimed structure of claim 1 above except explicitly stating that the source terminal layer, the gate terminal layer, and the drain terminal layer are respectively formed of metallized layers.

Herbert teaches (fig. 1) the use of metallic contacts as terminals to source electrode, drain electrode and gate electrode.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the metallic terminal taught Herbert in the structure of Yoshida in order to improve ohmic contact between the electrodes and the terminals.

The limitation of the metallized layers evaporated onto the source electrode, the gate electrode, and the drain electrode is considered a product-by-process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a

product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

7. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Okazaki et al., JP patent No. 06-326365.

Regarding claim 4, Yoshida teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the surfaces of the source terminal layer, the gate terminal layer, and the drain terminal layer are respectively formed with brazing layers.

It is conventional and also taught by Okazaki (figs. 1A and B) the use of brazing (soldering) material to form terminals (3 and 4) in a structure of a semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a brazing (soldering) material to form the surfaces of the source terminal layer, the gate terminal layer, and the drain terminal layer as taught by Okazaki in the structure of Yoshida in order to reduce the process cost.

Regarding claim 5, Yoshida teaches substantially the entire claimed structure of claim 1 above except explicitly stating a circuit board, wherein the power MOSFET is packaged in such a manner that the respective main surfaces of the semiconductor substrate in the power MOSFET are substantially normal to a circuit board.

Okazaki teaches an arrangement where a semiconductor device (refer to fig. 1B) is situated on a substrate (8) wherein the semiconductor device is packaged in such a

manner that the respective main surfaces of the semiconductor device are substantially normal to the substrate (8, refer to fig. 1B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the MOSFET of Yoshida in such a manner that the respective main surfaces of the semiconductor substrate in the MOSFET are substantially normal to a circuit board as taught by Okazaki in order to form a miniaturized thin type power MOSFET structure.

Regarding claim 6, Yoshida teaches substantially the entire claimed structure of claims 1 and 5 above including the source terminal layer, the gate terminal layer, and the drain terminal layer in the power MOSFET are respectively brazed (soldered) to the circuit board (substrate 8) with brazing (soldering) materials (refer to fig. 1B of Okazaki).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida, Okazaki and in view of Bencuya et al. US patent No. 6,423,623.

Yoshida teaches substantially the entire claimed structure of claims 1 and 5 above except explicitly stating that an encapsulating resin material is provided so as to cover the semiconductor substrate, the source terminal layer, the gate terminal layer, and the drain terminal layer in the power MOSFET.

Bencuya teaches using a resin material (molding material 300, fig. 3) to provide packaging to a power MOSFET device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packaging taught by Bencuya in the structure of Yoshida in order to provide a package that reduces package resistances.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and C are cited as being related to power MOSFET packaging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
April 11, 2005

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SUPERVISORY PATENT EXAMINER
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